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Research Project

van der Waals 2D semiconductor nanostructures with superconducting contacts

Third-party funded project

Project title van der Waals 2D semiconductor nanostructures with superconducting contacts

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Project start 01.02.2018

Probable end 31.01.2022

Status Completed

The combination of semiconducting nanostructures with standard superconducting materials hold great promises for finding new physical phenomena, as well as for applications in quantum information processing. Currently, strong efforts are made to demonstrate and exploit Majorana bound states (MBSs), i.e. protected zero-energy states at the ends of a topologically non-trivial superconductor. The latter is obtained by combining one-dimensional (1D) semiconducting nanowires (NWs) with a large spin-orbit interaction (SOI) with conventional superconductors. In very similar electronic devices our group already demonstrated Cooper pair splitting (CPS) [5,6], believed to be a source of spatially separated entangled electrons. However, these 1D systems are strongly limiting the device geometry and scalability, because the NWs are deposited randomly and have a considerable height, which makes the fabrication of thin superconducting contacts challenging. While standard semiconducting heterostructures like AlGaAs/AIAs are difficult to combine with superconducting or ferromagnetic contacts, graphene is a more versatile platform, but lacks the energy gap necessary for simple gate confinement, and has only a small SOI. Other 2D layered materials (LMs), like MoS₂ or WSe₂, have a large SOI, exhibit appreciable energy gaps, can have good transport properties [9] and can probably be contacted by thin metal contacts, all of which makes them ideal candidates for scalable and complex electronic devices based on SOI and superconductivity.

The general aim of this project is to develop a semiconductor electronics platform based on large-SOI 2D layered materials, which allow us to obtain quantum confinement by electrical gating and a strong coupling to metallic superconductors and ferromagnetic materials. We will develop two specific device types: A) Majorana and Parafermion devices, and B) gate-defined quantum dots (QDs), in four project phases summarized below.

Keywords semiconductors, superconductors, nanoelectronics

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Public Administration

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